

CLAIMS

1. A method for improving access latency of multiple bank devices, the method comprising the steps of:

identifying a plurality of different memory banks of a shared resource;

5 identifying a logical memory address map of a processor accessing the shared resource; and

mapping the logical memory address map to a shared resource address map wherein each memory address of the logical memory address is distributed through the plurality of different memory banks.

10 2. The method of claim 1, wherein each memory address of the logical memory address map accesses each of the plurality of memory banks.

3. The method of claim 1, wherein each access of each of the plurality of different memory banks overlaps each other.

4. The method of claim 1, wherein bursting cycles are not interfered.

15 5. The method of claim 4, wherein the bursting cycles include efficient transfers of small sequential streams of data to a same memory bank.

6. The method of claim 1, wherein interleave accesses are improved.

7. The method of claim 1, wherein the plurality of memory banks comprise at least four different memory banks.

20 8. The method of claim 1, wherein the shared resource comprises one or more of DRAM, SDRAM and DDR.

9. The method of claim 1, wherein the step of mapping further comprises the step of:

exchanging higher order address lines with mid-order address lines.

25 10. The method of claim 1, wherein the processor's local code is spread across the plurality of memory banks.

11. A system for improving access latency of multiple bank devices, the system comprising:

30 an identifying memory banks module for identifying a plurality of different memory banks of a shared resource;

an identifying address map module for identifying a logical memory address map of a processor accessing the shared resource; and

a mapping module for mapping the logical memory address map to a shared resource address map wherein each memory address of the logical memory address is distributed through the plurality of different memory banks.

12. The system of claim 11, wherein each memory address of the logical memory address map accesses each of the plurality of memory banks.

13. The system of claim 11, wherein each access of each of the plurality of different memory banks overlaps each other.

14. The system of claim 11, wherein bursting cycles are not interfered.

15. The system of claim 14, wherein the bursting cycles include efficient transfers of small sequential streams of data to a same memory bank.

16. The system of claim 11, wherein interleave accesses are improved.

17. The system of claim 11, wherein the plurality of memory banks comprise at least four different memory banks.

18. The system of claim 11, wherein the shared resource comprises one or more of DRAM, SDRAM and DDR.

19. The system of claim 11, wherein the mapping module further exchanges higher order address lines with mid-order address lines.

20. The system of claim 11, wherein the processor's local code is spread across the plurality of memory banks.

21. The method of claim 1, wherein the steps are performed at a customer premise equipment.

22. The method of claim 1, wherein the steps are performed at a central office.

23. The system of claim 11, wherein the system comprises a customer premise equipment.

24. The system of claim 11, wherein the system comprises a central office.

25. A computer readable medium, the computer readable medium comprising a set of instructions for improving access latency of multiple bank devices and being adapted to manipulate a processor to:

- identify a plurality of different memory banks of a shared resource;
 - identify a logical memory address map of a processor accessing the shared resource; and
 - map the logical memory address map to a shared resource address map wherein
- 5 each memory address of the logical memory address is distributed through the plurality of different memory banks.